In the Abstract:

~~Field-effect transistor, associated use and associated fabrication method~~

~~An explanation is given of a~~A vertical field-effect transistor having a semiconductor layer ~~(10)~~, in which a doped channel region is arranged along a depression ~~(72)~~. A "buried" terminal region ~~(18, 54)~~ leads as far as a surface of the semiconductor layer ~~(10)~~. ~~The field-effect transistor has outstanding electrical properties and is simple to fabricate.~~ The field-effect transistor also has a doped terminal region near an opening of the depression as well as the doped terminal region remote from the opening, a control region arranged in the depression, and an electrical insulating region between the control region and the channel region. The terminal region remote from the opening leads as far as a surface containing the opening or is electrically conductively connected to an electrically conductive connection leading to the surface. The control region is arranged in only one depression. The field-effect transistor is a drive transistor at a word line or at a bit line of a memory cell array.

~~(Figure 1C)~~